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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,959	07/30/2001	Tomoyuki Taguchi	JP920000005US1 (14606)	9354

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EXAMINER	
CHAN, EMILY Y	
ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/917,959	Applicant(s) TAGUCHI, TOMOYUKI	
	Examiner emily y chan	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *53* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *22 May 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1) Claims 1-16 remain for examination.

2) The rejection under 35 U.S.C. 102 (b) as being anticipated by Suzuki et al ('030) for claims 1-2 and 13-14 dated on 2/20/03 is withdrawn.

3) A new rejection ground is given as follows.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al ('030) in view of Tomitam ('061).

Suzuki et al ('030) disclose an inspection method for an array substrate as claimed (see fig 7) below, in which the array substrate comprises: a substrate (5); a plurality of gate lines (26); a plurality of signal lines (28); a plurality of common power source terminal line (33); a plurality of switching elements (6, 30) electrically connected respectively to the a plurality of gate lines (26) and to the a plurality of signal lines (28); and a plurality of storage capacitors (8) electrically connected respectively to the plurality of common power source terminal line (33) and to the plurality of switching elements (6) (see 5, lines 30-35). Suzuki et al ('030) expressly teach (see col. 7, lines 12-20 and col. 11, lines 1-5) that:

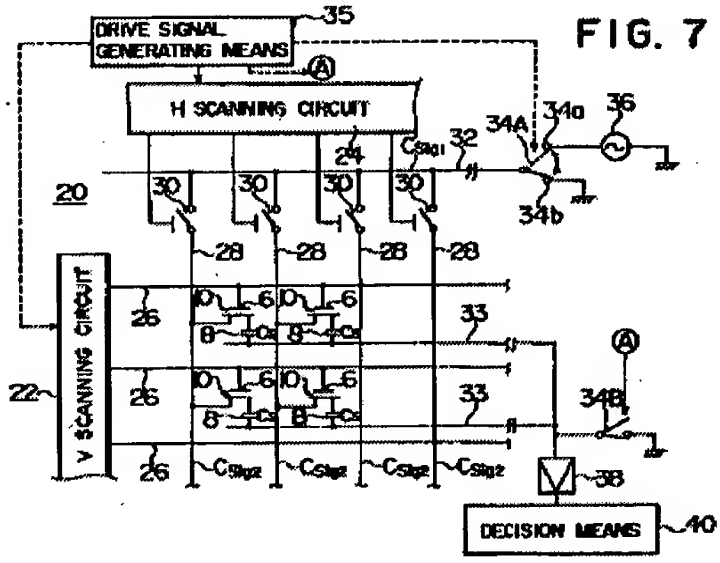


FIG. 7

(1) Applying voltage from the plurality of common power source terminal lines (33) to the plurality of storage capacitors (8) (See Col. 7, lines 14-16 " the voltage from the common power source terminal line 33 is applied to the capacitor element 8");

(2) Applying voltage signal (V1) from the plurality of signal lines (28) to the plurality of storage capacitors (8) via a plurality of switching elements (6, 30); and

(3) Measuring quantities of charge stored in the storage capacitors (8) by a circuit (40) (see Col. 7, lines 51-55) based on potential difference between the two voltage signals (V1 and " voltage from the common power source terminal line 33" (see col. 7, lines 12-20, 35-38 and lines 52-55).

Suzuki et al ('030) does not teach the step of applying pulse signals from a plurality of storage capacitor lines to the plurality of storage capacitors.

Tomitam ('061) discloses a testing method for a substrate of active matrix display panel and expressly teaches that a pulse signal is applied from a plurality of storage capacitor lines (52) to a plurality of storage capacitors (61) (see Col. 9, lines 20-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of applying pulse signals through the storage capacitor lines to the storage capacitors as taught by Tomitam ('061) into Suzuki et al ('030)'s method for the purpose of locating or inspecting a defect pixel in the array substrate to improve the product yield and a reliability as disclosed by Tomitam ('061) (see col. 2, lines 20-23 and lines 65-67).

With respect to claim 3,Tomitam ('061) teaches that a pulse signal 20V applied from a plurality of storage capacitor lines (52) to plurality of storage capacitors (61) and a pulse signal 5V from a plurality of signal lines (X) to plurality of storage capacitors (61) are simultaneously applied to the plurality of storage capacitors (61) (see Col, 9, lines 20-25).

With respect to claims 4-6, because Tomitam ('061) does not specify that the rising times of the two pulse signals (5V and 20V) are the same, therefore, it would have been obvious to one of ordinary skill in the art that the rising times are different.

With respect claims 7and 9, Suzuki et al ('030) teach that the quantities of charges stored in only one single storage capacitor (8) among the plurality of storage capacitors (8) electrically connected to the common power source terminal line (33) is measured (see col. 3, line 27 "so accurate inspection of each pixel is possible" and Col. 13, line 43, " each pixel corresponds to a capacitor").

With respect to claims 8, 10, Suzuki et al ('030) teach that the measuring of the quantity of charges stored in the only one single storage capacitor (8) is performed for all of the plurality of common power source terminal lines (33) (See col. 3, lines 11-13).

With respect to claims 11-12, Suzuki et al ('030) teach that wherein in the measuring step, the quantities of charges stored in the plurality of storage capacitors (8) connected to the signal lines (28) via the plurality of switching elements (6, 30) are measured (see col.7 and Fig 2).

Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al ('030) in view of Tomitam ('061).

Suzuki et al ('030) expressly teach an inspection device for an array substrate as claimed (see fig 7), in which the array substrate comprises: a substrate (5); a plurality of gate lines (26); a plurality of signal lines (28); a plurality of common power source terminal line (33); a plurality of switching elements (6, 30) electrically connected respectively to the a plurality of gate lines (26) and the a plurality of signal lines (28); and a plurality of storage capacitors (8) electrically connected respectively to the plurality of common power source terminal line (33) and to the plurality of switching elements (6) (see 5, lines 30-35). Suzuki et al ('030)' inspection device comprises

A pulse signal generating device (36) connected to the signal lines (28) in order to apply the pulse signals respectively to the plurality of storage capacitors (8); and

A circuit (40) for measuring the quantities of charges stored in the respective plurality storage capacitors (8) (See Col. 7, lines 51-55).

Suzuki et al '(030) do not teach a pulse signal generating device connected to a plurality of storage capacitor lines in order to apply the pulse signals respectively to the plurality of storage capacitors (8).

Tomitam ('061) discloses a testing method for a substrate of active matrix display panel and expressly teaches a storage capacitance line driving circuit 21 to apply a pulse signal through a plurality of storage capacitor lines (52) to a plurality of storage capacitors (61) (see Col. 4, line 14 and Col. 9, lines 20-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Tomitam ('061)' s pulse signal generating device (21) for applying pulse signals through the storage capacitor lines to the storage capacitors into Suzuki et al ('030)'s device for the purpose of locating or inspecting a defect pixel in the array substrate to improve the product yield and a reliability as disclosed by Tomitam ('061) (see col. 2, lines 20-23 and lines 65-67).

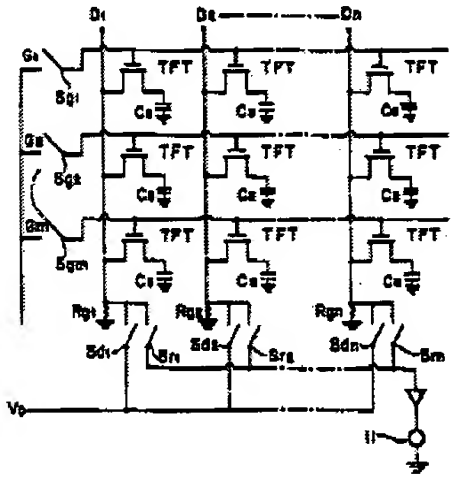
Claims 15-16 rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al ('030) in view of Tomitam ('061) as applied to claims 13-14 above, and further in view of Takahashi et al ('300).

Suzuki et al ('030) and Tomitam ('061) do not teach the measuring circuit (40) for measuring the quantities of charges stored in said storage capacitors is connected to the signal lines (28).

Takahashi et al ('300) disclose a method and apparatus for testing TFT-LCD and expressly teach a circuit (waveform analyzer 11) for measuring the quantities of

discharge released from the storage capacitor (see Fig 10 below) is connected to signal lines (D1...Dn) through relays (Sr1...Srn).

FIG. 10



It would have been obvious to one of ordinary skill in the art at the time the invention as made to incorporate the teaching of Takahashi et al ('300)' measuring circuit connected to the signal lines into Suzuki et al ('030) in view of Tomitam ('061)' s device, because by using a relay, whether or not the TFTs corresponding to the individual pixels are properly connected can be determined efficiently as disclose by Takahashi et al ('300) (see col. 6, lines 25-30).

Applicant's arguments with respect to claims 1-2 and 7-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily y Chan whose telephone number is 7033056123. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Cuneo Kammie can be reached on 7033081233. The fax phone numbers for the organization where this application or proceeding is assigned are 7033085841 for regular communications and 7033085841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 7022056123.

EC
July 25, 2003

VINH P. NGUYEN
PRIMARY EXAMINER
GROUP 2829
07/28/03